signal[[,]] so as to cause one of the row drive signals to be outputted to a first output terminal.

10. (Withdrawn) A display device, comprising:

a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner;

a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines connected to the pixels, in accordance with the row drive timing signal;

a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and

a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

the row drive circuit being arranged such that, driver ICs are disposed in accordance with a system-on-film structure, a line passing under an IC chip of predetermined one of the driver ICs is connected to an output terminal next to

an output terminal corresponding to a last one of the row lines of said predetermined one of the driver ICs, and the line passing under the IC chip is provided before a first one of the row lines provided on the display panel, acting as a dummy row line.

11. (Currently Amended) A control device of a display drive circuit, wherein,

the display drive circuit includes: a row drive circuit which receives a row drive timing signal which is for driving row lines of a display panel on which pixels corresponding to respective intersections of the row lines and column lines are provided in a matrix manner, and serially outputs row drive signals, which are for driving the row lines, to the respective row lines connected to the pixels, in accordance with the row drive timing signal; and a column drive circuit which receives display data and a column drive timing signal which is for driving the column lines of the display panel, and outputs column drive signals, which correspond to the display data, to the respective column lines connected to the pixels, in accordance with the column line drive timing signal,

the control device receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and supplies the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and supplies the <u>colum drive timing signal</u> ~~clock signal~~ to the column drive circuit, along with the display data[[,]]; [[and]]

~~during a period from the~~ the control device generates the row drive timing signal with reference to a timing of inputting the data enable signal and supplies the row drive timing signal, which has been generated, to the row drive circuit, so that ~~to a start of outputting the column drive signals of a first horizontal period of one vertical period, the control device generates the row drive timing signal with reference to a timing of inputting the data enable signal, in order to cause~~ one of the row drive signals [[to be]] is supplied to a first output terminal of the row drive circuit during a period from the timing of inputting the data enable signal to a start of the column drive circuit outputting the column drive signals of a first horizontal period of one vertical period; and~~, and then supplies the row drive timing signal, which has been generated, to the row drive circuit~~

the row drive timing signal includes: a pulse shifted start pulse signal for determining timings to serially output the row drive signals to respective row lines; and a shift clock signal for determining a timing to shift the start pulse signal.

12. (Currently Amended) A driving method of a display device, wherein:

the display device includes: a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner; a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines

connected to the pixels, in accordance with the row drive timing signal; a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

the display data, a data enable signal, and a clock signal are received, the row drive timing signal is generated from the data enable signal and the clock signal and supplied to the row drive circuit, and the column drive timing signal is generated from the data enable signal and the clock signal and supplied to the column drive circuit, along with the display data, and

the row drive timing signal is generated with reference to a timing of inputting the data enable signal and supplied to the row drive circuit, so that one of the row drive signals is supplied to a first output terminal of the row drive circuit during a period from the timing of inputting the data enable signal to a start of the column drive circuit outputting the column drive signals of a first horizontal period of one vertical period[[,]]; and

the row drive timing signal includes: a pulse shifted start pulse signal for determining timings to serially output the row drive signals to respective row lines; and a shift clock signal for determining a timing to shift the start pulse signal ~~is generated with reference to a timing of inputting the data enable signal, in order to cause one of the row drive signals to be supplied to a first output terminal of the row drive circuit, and then the row drive timing signal, which has been generated, is supplied to the row drive circuit~~.